Total No. of Questions : 09

B.Tech. (IT) (2018 Batch) (Sem.–3)
COMPUTER ARCHITECTURE
Subject Code : BTES-302-18
M.Code : 76394

Time : 3 Hrs.   Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Answer briefly :**

   a. What is Structural hazard in pipelining?

   b. Differentiate between 1's complement and 2's complement number representation systems.

   c. What are maskable and non-maskable interrupts?

   d. Differentiate between magnetic disks and magnetic tapes.

   e. Explain pros and cons of CISC architecture.

   f. Define Microinstruction and Microoperation.

   g. Write brief note on USB.

   h. Define Cache hit and cache miss.

   i. What are privileged and non-privileged instructions?

   j. What is Cache coherency?

SECTION-B

2. Explain Interrupt and DMA mode for I/O access.

3. Explain booth multiplier in detail.

4. Explain in brief :

   a. Accumulator machine

   b. Stack machine

5. Explain components of instruction cycle.

6. Discuss PC relative and Base register addressing mode

SECTION-C

7. Explain various stages in instruction pipelining. Discuss in detail methods to handle Data hazards.

8. Explain below page replacement algorithms with examples :

   a. FIFO

   b. LIFO

   c. Least recently used

   d. Optimal Page replacement

9. Give the hardware organization of associative memory. Why associative memory is faster than other memories? Deduce the logic equation used to find the match in the associative memory.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.